IFW

Docket No.: 101-1019

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:

Hyun-kyu YUN

Application No.:	10/808,341	Group Art Unit No.:	2189
Filed:	March 25, 2004	Examiner	Woo H. CHOI
Customer No.:	38209	Confirmation No.	5441

For: DSP (DIGITAL SIGNAL PROCESSING) ARCHITECTURE WITH A WIDE MEMORY BANDWIDTH AND A MEMORY MAPPING METHOD THEREOF

RESPONSE TO RESTRICTION REQUIREMENT

Assistant Commissioner for Patents
Alexandria, Virginia 22313

Sir:

The Examiner has issued a Notice of Non-responsive Reply, dated November 28, 2007, advising that Applicant's Response of October 18, 2007 did not include an Election from the Restriction Requirement, dated September 10, 2007. It is respectfully submitted that an Election is made difficult due to the unclear reasoning in the Restriction Requirement. However, for purposes of being fully responsive only, Applicant provisionally elects Group I, with traverse, and request that the Restriction Requirement be withdrawn, for at least the reasons discussed below.

It is respectfully submitted that the Examiner has required restriction three times thus far during the prosecution of the subject patent application. In the first Restriction Requirement, dated March 27, 2006, claims 1-6 and 11-16 were assigned to the same Group, and Applicant elected that Group without traverse. The Examiner considered claims 1-6 and 11-16 together. In the second Restriction Requirement, dated November 30, 2006, claims 1-6 and 11-16 were once again grouped together, although the Examiner failed to include claims 17-18 in any of the Groups. Applicant elected the group containing claims 1-6 and 11-18, once again without traverse. These claims were once again considered together and finally rejected. Applicant responded with an amendment after final, which was entered upon filing a Request for Continued Examination on June 20, 2007. Now, the Examiner contends that "the inventions have

acquired a separate status in the art," and that "the inventions require a different field of search." However, Applicant respectfully submits that errors exist in the classification of Applicant's inventive concept, as is discussed in the paragraphs that follow.

It is respectfully submitted that the Examiner has misclassified Group I, in that class 711/173 is not only directed to memory, whereas the inventive concept of the subject patent application is clearly a processor architecture, but is directed specifically to **partitioning logical memory**, which has nothing to do with the present general inventive concept. Even a casual perusal of the specification and claims of the subject patent application reveals that the memory within the DSP architecture implements physical memory and is not limited to any logical memory partition used therewith. Thus, it is respectfully submitted that for at least the reason that the claims of Group I are misclassified, a *prima facie* necessity to restrict Group I from the other claims of the subject patent application has not been shown.

The Examiner contends that claims 11 and 17 of Group II must be searched under class 711/149, which allegedly imparts a serious burden on the Examiner. It is to be noted that class 711/149 is directed to means or steps for controlling shared memory capable of supporting a plurality of simultaneous read accesses. Nowhere is a limitation of simultaneous read access of a memory unit recited in the claims of Group II, and thus the claims of Group II are misclassified also. For at least the reason that the claims of Group II are misclassified, a *prima facie* necessity to restrict Group II from the other claims of the subject patent application has not been shown. Additionally, it is respectfully submitted that claim 11, which stands as originally presented, and claim 17, which has not been amended since the last election, have both been allowed as previously examined.

In the Restriction Requirement, the Examiner further contends that Group II, directed to claims 11 and 17, which have already been allowed by the Examiner, is distinct from the other inventions since "**none of the structures** of the other inventions **require the use of two different ports to store data in a column or row direction** as claimed in invention II. The structures can be used to store data through one port in one direction only or though [sic] one or more ports in no particular direction," (emphases added). *See* Detailed Action, page 3, item 2. The Examiner further states that "[p]hysical configuration of III, of **having a middle row connected to one port** and **middle column connected to another port** is also **quite distinct** from the other two inventions [I and IV]," (emphases added). *See* Detailed Action, page 3, item 3. It is

respectfully submitted that, regardless of whether certain of these claims include process steps and others include recitations of concomitant structure, there is contradiction where the Examiner first states that none of the other allegedly distinct inventions is like that of Group II, since they do not use two different ports to store data in a row or column, and then states that Group III is distinct because it implements two different communication ports connected to, respectively, a row and a column. Thus, it is respectfully submitted that, given the misclassification of Group II and the afore-discussed contradictions, a *prima facie* necessity to restrict Group III from the other claims of the subject patent application has not been shown.

Additionally, the Examiner contends that the claims of Groups III, which the Examiner states is drawn to a DSP apparatus for motion picture data and allegedly classified in class 712/11, "Subject matter including details of a structure which mutually joins the identical processing elements," and Group IV, which the Examiner states is drawn to a digital processing apparatus with a communication port to provide image frames, and allegedly classified in class 712/14, "Subject matter which controls the structure joining the memory within an individual array processor element or associated with an individual array processor element," require restriction, one from another. The Examiner states that Group IV is allegedly usable in a non-matrix configuration, but does not clarify how such is different from the recitations of Group I other than "subcombinations I and IV have separate utility such as for use process images other than motion pictures." However, claims 31-33 of Group IV recite no limitation as to data type, and no evidence has been provided by the Examiner how these claims have separate utility from the claims of Group I. Thus, for at least this additional reason, a *prima facie* necessity to restrict at least claims 31-33 from the other claims of the subject patent application has not been shown.

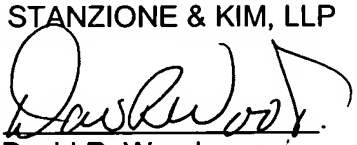
It is respectfully submitted that the Examiner has not shown a *prima facie* necessity to restrict the claims into the Groups I-IV, and it is therefore requested that examination of the subject claims on the merits proceed in a single group, for at least the reason that no **clear evidence** has been provided to indicate that a **serious** burden would exist if the claims remained together. As set forth in MPEP § 803, "[if] the search and examination of all the claims in an application can be made without serious burden, the examiner must examine them on the merits, even though they include claims to independent or distinct inventions."

Thus, as stated above, for purposes of being fully responsive to the Restriction Requirement only, Applicant provisionally elects Group I, and respectfully requests that, for at least the reasons discussed above, the Restriction Requirement be withdrawn.

Respectfully submitted,

STANZIONE & KIM, LLP

Date: December 27, 2007

By: 

David R. Wood
Registration No.: 53,868

Stanzione & Kim, LLP
919 18th St., NW, Suite 440
Washington, DC 20006
Telephone: 202-775-1900
Facsimile: 202-775-1901